TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. BUR920000143US1

In Re Application Of: **Douglas D. Coolbaugh, et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/773,798	February 1, 2001	Dana Farahani	2814

Invention: **NITRIDE PASSIVATION FOR IMPROVED BIPOLAR YIELD**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **March 1, 2004.**

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Dated: **May 3, 2004**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Douglas D. Coolbaugh, et al. Examiner: Dana Farahani

Serial No: 09/773,798 Art Unit: 2814

Filed: February 1, 2001 Docket: BUR920000143US1 (13890)

For: NITRIDE PASSIVATION FOR IMPROVED BIPOLAR YIELD Dated: May 3, 2004

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APPELLANTS' BRIEF ON APPEAL

1. Real Party in Interest

The real party in interest of the present application is International Business Machines Corporation, the assignee of the entire right, title and interest in the above-identified patent application.

2. Related Appeals and Interferences

No other appeals or interferences are known which directly affect, or will be directly affected by, or have a bearing on, the disposition of the pending appeal.

3. Status of the Claims

The present application was filed on February 1, 2001 with Claims 1-17. A first Office Action on the merits issued December 19, 2001, to which Appellants filed an Amendment and Response, dated March 19, 2002. In the March 19, 2002 Amendment & Response, Appellants amended Claims 1, 7, and 9. In response to a second Office Action dated May 3, 2002, Claim 9 was amended for a second time in Appellants' Response,

dated July 31, 2002. A Final Rejection issued on October 15, 2002. In response to the Final Rejection, Appellants filed a Response under 37 C.F.R. §1.116, dated December 16, 2002, in which there were no amendments to the claims. An Advisory Action was issued on January 21, 2003, in which the Examiner maintained the rejection of Claims 1-17. A Request for Continued Examination (RCE) was filed on February 19, 2003, in which, Appellants submitted a Response, wherein Claim 1 was amended for a second time, Claim 9 was amended for a third time, and new Claim 18 was added.

In response to an Office Action that issued on May 20, 2003 in the RCE, Appellants filed a Response dated August 20, 2003. A Final Rejection was issued on November 28, 2003. In response to the Final Rejection dated November 28, 2003, Appellants filed a Response under 37 C.F.R. §1.116, dated January 27, 2004, in which Claims 1, 9 and 18 were amended.

Appellants filed a Notice of Appeal on March 1, 2004. An Advisory Action was issued on March 5, 2004, in which the amendments to Claims 1, 9, and 18 made in Appellants' Response, dated January 27, 2004, were entered for consideration on Appeal. Thus, Claims 1-18 are the subject of this appeal; these claims, as they presently stand, are set forth in the Appendix of this Appeal Brief. The status of each of the claims is thus as follows:

Claims 1-18: Finally rejected and on appeal.

4. Status of the Amendment

A Response to the Final Rejection dated November 28, 2003 containing amendments to Claims 1, 9, and 18 was filed on January 27, 2004. These amendments were entered, as of record, in the Advisory Action issued on March 5, 2004.

5. Summary of Invention

The invention embodied by Claims 1-18, on appeal, relates to a SiGe heterojunction bipolar transistor, as illustrated in FIG. 2, and a method of forming a SiGe heterojunction bipolar transistor, as illustrated in FIGS. 3-8. The inventive SiGe heterojunction bipolar transistor comprises a semiconductor substrate 50 having a collector 56 and subcollector region 54 located therein, wherein the collector 56 is located between isolation regions 52 that are also present in the substrate 50; a SiGe layer 62 atop the substrate 50, the SiGe layer 58 including polycrystalline Si regions positioned above the isolation regions 52 and a SiGe base region 62 located above the collector 56 and subcollector regions 54; a patterned insulator layer 64 atop the SiGe base region 62, the patterned insulator 64 having an opening therein; an emitter 66 located on the patterned insulator layer 64 and in contact with the SiGe base region 62 through the opening, the emitter 66, the patterned insulator layer 64 and the SiGe base region 62 each having exposed sidewalls; a permanent conformal passivation layer 68 positioned on the exposed sidewalls of the emitter 66, the patterned insulator layer 64 and a portion of the SiGe base region 62; and silicide regions 70 located on exposed portions of the SiGe layer 58, including portions of the SiGe base region 62, and the emitter 66 not covered by the permanent conformal passivation layer 68, wherein the permanent passivation layer 68 prevents bridging between silicide regions 70 thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%. In one embodiment of the present invention, the permanent conformal passivation layer 68 is positioned on the exposed sidewalls of the emitter 66, the patterned insulator layer 64 and an inclined portion of the SiGe base region 62.

Another aspect of the present invention is a method of forming the above-described SiGe heterojunction bipolar transistor. The inventive method for fabricating a SiGe heterojunction bipolar transistor comprises the steps of providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region 62, an insulator layer 64 formed on surface portions of the underlying SiGe base region 62, and an emitter 66 formed on the insulator layer 64 and in contact with the underlying SiGe base region 62 through an emitter opening formed in the insulator layer 64, the emitter, the insulator layer 64 and the SiGe base region 62 each having exposed sidewalls; forming a permanent passivation layer 68 on the exposed sidewalls of the emitter 66, the insulator layer 64 and portions of the SiGe base region 62; and siliciding exposed silicon surfaces of at least the emitter 66 and the SiGe base region 62 not protected by the permanent passivation layer 68 to form silicide regions 70 therein, wherein the permanent passivation layer 68 prevents bridging between silicide regions 70 thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.

6. Issues on Appeal

I. Do the combined disclosures of Appellants' admitted prior art ("AAPA"), U.S. Patent No. 5,177,567 to Klersy, et al. ("Klersy, et al.") and SEDRA & SMITH, MICROELECTRONIC CIRCUITS (4^{TH} Ed 1998) ("Sedra and Smith") render Claims 1, 9, 13, 14, 15 and 18, on appeal, unpatentable under 35 U.S.C. §103(a)?

II. Do the combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 6,331,492 to Misium, et al. ("Misium, et al.") render Claims 2 and 5-8, on appeal, unpatentable under 35 U.S.C. §103(a)?

III. Do the combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 4,987,102 to Nguyen, et al. ("Nguyen, et al.") render Claims 3, 4, 16, and 17, on appeal, unpatentable under 35 U.S.C. §103(a)?

IV. Do the combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 4,757,027 to Vora ("Vora") render Claims 10 and 11, on appeal, unpatentable under 35 U.S.C. §103(a)?

V. Do the combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 6,268,779 to Van Zeijl ("Van Zeijl") render Claim 12, on appeal, unpatentable under 35 U.S.C. §103(a)?

7. Grouping of the Claims

The claims involved in Issue I stand and fall together.

The claims involved in Issue II stand and fall together.

The claims involved in Issue III stand and fall together.

The claims involved in Issue IV stand and fall together.

Issue V relates to a single claim.

8. Arguments for Patentability

I. The combined disclosures of Appellants' admitted prior art ("AAPA"), Klersy, et al. and Sedra and Smith do not render Claims 1, 9, 13, 14, 15 and 18, on appeal, unpatentable under 35 U.S.C. §103(a).

In the Final Rejection dated November 28, 2003, Claims 1, 9, 13, 14, 15 and 18 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over the combination of

Appellants' admitted prior art ("AAPA"), Klersy, et al. and Sedra and Smith. Appellants respectfully disagree with the Examiner's conclusion that the combination of the AAPA, Klersy, et al. and Sedra and Smith render Appellants' invention obvious and submit the following.

To establish a prima facie case of obviousness, under 35 U.S.C. §103, three criteria must be met. First there must be some suggestion or motivation, either in the references themselves or the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references) combined must teach or suggest all of the claimed limitations. *See Hodosh v. Block Drug Co., Inc.,* 786 F.2d 1136, 1143, 229 USPQ 182, 187 (Fed. Cir. 1986).

Appellants respectfully submit that the Examiner has failed to produce a prima facie case of obviousness of Claims 1, 9, 13, 14, 15 and 18 over the applied references, since the applied references fail to teach or suggest all of the claimed limitations of Appellants' invention. Specifically, the combined disclosures of the AAPA, Klersy, et al. and Sedra and Smith do not teach or suggest a heterojunction bipolar structure or fabrication method wherein a permanent passivation layer is present which *prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%*, as recited in Claims 1, 9 and 18. Further, there is no suggestion or motivation, either in the references themselves or the knowledge generally available to one of ordinary skill in the art, to modify the reference teachings to produce Appellants' claimed invention. Appellants' arguments are now discussed in greater detail.

a. Appellants' claimed heterojunction bipolar structure or fabrication method is not obvious over the combined disclosures of the AAPA, Klersy, et al. and Sedra and Smith, since the applied prior art fails to teach or suggest each and every limitation of Appellants' heterojunction bipolar structure or fabrication method, as recited in Claims 1, 9 and 18, on appeal.

Appellants respectfully submit that the combined disclosure of the AAPA, Klersy, et al. and Sedra and Smith fail to render the Appellants' invention obvious, since the combined prior art does not teach or suggest a heterojunction bipolar structure, or fabrication method, comprising a permanent passivation layer that prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%, as recited in Claims 1, 9 and 18, on appeal. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Appellants have determined that bipolar yield may be increased by forming a permanent dielectric passivation layer on the edges of the emitter prior to silicidation of the source/drain regions and the gate region. During silicidation, silicide material does not form on the permanent dielectric passivation layer, since silicide only forms on Si-containing materials. Therefore, the permanent dielectric passivation layer prevents bridging between silicide regions on the emitter and the SiGe body, thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.

The AAPA shown in FIG. 1 of the present application is defective since it fails to teach or suggest a permanent conformal passivation layer formed on the exposed sidewalls of

an emitter. AAPA discloses a heterojunction bipolar transistor structure, which does not include a conformal passivation layer. The heterojunction bipolar transistor structure, as disclosed in AAPA, typically results in a 20-30% bipolar yield loss. *See* Page 2, lines 5-6, of Appellants' specification. The loss associated with the SiGe bipolar transistor structure, as disclosed in AAPA, is attributed to the presence of silicide bridges between the emitter and SiGe body, which introduce shorts to the structure during silicidation. Appellants' claimed structure and method utilize a permanent conformal passivation layer to avoid the formation of silicide bridges and losses associated with prior art devices.

The defect associated with AAPA is not alleviated by the disclosure of Klersy, et al., since the applied secondary reference does not teach or suggest that by forming a permanent passivation layer on the emitter prior to silicidation one can prevent the bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%. Klersy, et al. provide a thin-film structure for solid state thin-film electrical switching devices which includes a passivation layer that is deposited over the thin-film structure. In accordance with Col. 10, lines 30-34, Klersy, et al. disclose that the passivation layer provides protection against environmental contamination and/or unintended electrical contact with other devices or circuits.

The Klersy, et al. disclosure does not teach, suggest or insinuate that forming a permanent passivation layer prior to silicidation can prevent bridging between silicide regions, thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%. Specifically, the combined affects of short prevention and bipolar yield are not taught or suggested in Klersy, et al.

Further, Klersy, et al. do not include a bipolar emitter and therefore could not have recognized that by forming a permanent passivation layer on the emitter prior to silicidation one can prevent the bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%

Sedra and Smith do not fulfill the deficiencies of AAPA and Klersy, et al. Sedra and Smith disclose a bipolar junction transistor consisting of three semiconductor regions; the emitter, the base region, and the collector region. *See* Page 222 of Sedra and Smith. Sedra and Smith fail to teach or suggest that by forming a permanent passivation layer on the emitter prior to silicidation one can prevent the bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%, as recited in Claims 1, 9 and 18.

Referring to the Advisory Action dated March 5, 2004, it is the Examiner's position that the claimed limitation that Appellants' permanent passivation layer prevents the bridging between silicide regions and thereby *substantially eliminating shorts and improving bipolar yield by as much as 20-30%* is inherent in the combined disclosures of the references. Appellants' respectfully disagree and submit the following.

Appellants reiterate that none of the applied prior art references disclose positioning a permanent passivation layer on the emitter prior to silicidation to prevent bridging between silicide regions. The Federal Circuit has held that inherency cannot be based on mere speculation. *See e.g., Continental Can Co. USA, Inc. v. Monsanto Co.,* 848 F.2d 1264, 1269, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). "Facts asserted to be inherent in the prior art must be shown by evidence from the prior art". *In re Dembiczak,* 175 F.3d 949, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Since none of the references disclose Appellants' positioning of

the permanent passivation layer on the emitter sidewalls prior to silicidation, there is no evidence within the referenced prior art that those structures substantially *eliminate shorting and result in a bipolar yield improvement by as much as 20-30%.*

Therefore, Appellants' permanent passivation layers ability to prevent bridging between the silicide regions and thereby *substantially eliminating shorts and improve bipolar yield by as much as 20-30%* is not inherent in the combined disclosures of the AAPA, Klersy, et al., and Sedra and Smith.

The foregoing remarks clearly demonstrate that the combined disclosures of AAPA, Klersy, et al. and Sedra and Smith fail to teach or suggest a heterojunction bipolar structure, or fabrication method, comprising a permanent passivation layer that prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.

In view of the above remarks, Appellants respectfully submit that the Examiner has failed to produce a prima facie case of obviousness, since the combined disclosures of the AAPA, Klersy, et al., and Sedra and Smith fail to teach or suggest every limitation of Appellant's heterojunction transistor or fabrication method, as recited in Claims 1, 9, and 18.

b. Appellants' claimed heterojunction bipolar structure or fabrication method is not obvious over the combined disclosures of AAPA, Klersy, et al. and Sedra and Smith, since there is no suggestion or motivation, either in the references themselves or the knowledge generally available to one of ordinary skill in the art, to modify the reference teachings to produce Appellants' claimed invention.

Appellants submit that there is no motivation to modify the disclosures of the AAPA, Klersy, et al. and Sedra and Smith to provide a heterojunction bipolar structure, or fabrication method, comprising a permanent passivation layer that prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%, as recited in Claims 1, 9 and 18, on appeal. The § 103 rejections are thus improper since the prior art does not suggest this dramatic modification. The law requires that a prior art reference provide some teaching, suggestion or motivation to make the modification. In re Vaeck, 947 F.2d 488, 493, 20 USPQ 2d 1438, 1442 (Fed. Cir. 1991).

It is the Examiner's position, referring to page 7 of the Final Rejection, dated November 28, 2003, that one of ordinary skill in the art would recognize the fact that a bipolar transistor when shorted between any of its terminals is not useable in many applications. The Examiner continues to allege that it is well know in the art that passivation layers are widely used as protection or insulating layers in semiconducting layer. The Examiner then alleges that motivation does not need to be explicitly stated when the reason to combine the references are obvious to one of ordinary skill in the art. Appellants respectfully disagree and submit the following.

A statement that modifications of the prior art to meet the claimed invention would have been "well within the ordinary skill of the art at the time the claimed invention was made" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima fascia case of evidence without some object reason to combine the teachings of the references. *Ex Parte Levengood,* 28 USPQ2d 1300 (Bd. Pat. App. and Inter. 1993), Al-Site Corp. v. VSI, Int'l Inc., 174 F.3d 1308, 50 USPQ 2d 1161 (Fed. Cir. 1999). The level of skill in the art cannot be relied upon

to provide the suggestion to combine references. *Al-site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999).

Appellants submit that the Examiner has not provided sufficient objective reasoning for one of ordinary skill in the art to modify the passivation layer disclosed in Klersy, et al. to produce Appellants' claimed structure. The test for obviousness is what the combined teachings of the references would have suggested to one or ordinary skill in the art to the extend that they are in analogous arts. *See In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). A prior art reference is analogous if the reference is in the field of Applicants' endeavor, or if not, the reference is reasonably pertinent to the particular problem with which the inventor was concerned. *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992).

It is the Examiner's position, referring to page 3 of the Final Rejection dated November 28, 2003, that it would have been obvious for one of ordinary skill in the art to modify AAPA with the passivation layer disclosed in Klersy, et al., to produce Appellants' claimed transistor, since it is well known within the art that for a transistor to be useable it should not be shorted between the base and the emitter. Appellants' submit that there is no motivation for one of ordinary skill in the art to modify a three terminal bipolar transistor to include a passivation layer utilized in a two terminal chalcogenide switching device because chalcogenide devices and bipolar transistors are not within the same field of endeavor and the Klersy, et al. reference is not reasonably pertinent to the problem in which Appellants were concerned. *See In re Oetiker*, 977 F.2d 1443, 1446 24 USPQ2d 1443, 1445 (Fed. Cir 1992).

Appellants observe that the present invention and the Klersy, et al. device both present switching devices, but submit the test for analogy is not simple classifications of

devices, but whether the similarities and differences in the structure and function of the devices indicate whether referenced patents where pertinent to the art in which the Appellants' invention dealt. *In re Ellis,* 476 F.2d 1370, 1372, 177 USPQ 526, 527, (CCPA 1973).

The court in *Wang Laboratories, Inc. v. Toshiba Corp.* 993 F.2d 185, 26 USPQ2d 1767 (Fed. Cir. 1993) held that a prior art reference to single in-line memory modules for installation in industrial controllers were not necessarily in the same field of endeavor as patent claims directed to single in-line memory modules for installation on printed circuit motherboards for use in personal computers. The court reasoned that the reference was in a different field of endeavor because it involved memory circuits in which modules of varying sizes may be added or replaced, whereas the claimed invention included compact modular memories. Additionally, the Federal Circuit reasoned that a holding of non-analogous art was supported by the fact that the claims for the single in line memory modules at issue utilized dynamic random access memory, where the single in-line memory modules of the prior art reference utilized static random access memories or read only memories. Dynamic random access memory and static random access or read only memories have differing structure and function.

The claimed bipolar transistor and the switching device disclosed in Klersy, et al. are non-analogous art. Similar to the devices considered by the Federal Circuit in *Wang Laboratories, Inc. v. Toshiba Corp.,* the claimed bipolar transistor and the chalcogenide switching device disclosed in Klersy, et al. have different structures and functions. As discussed above, a bipolar transistor comprises an emitter, base and collector and is a three terminal device, where the interaction between the emitter and base and their respective

terminals control the switching behavior of the device and provide multiple conduction states. An efficient bipolar transistor has an emitter region having a higher doping concentration than the base region and a base region having a higher doping concentration than the collector. In order for the bipolar transistor to switch 'on', and for current to flow across the emitter/base junction the voltage introduced to the base region (p-type base in pnp transistor) must cause the potential of the base region to be greater than the potential of the emitter region, thus forward biasing the emitter base junction.

The chalcogenide switching device disclosed in Klersy, et al. does not have the doped emitter, base and collector regions of a bipolar transistor. Klersy, et al. disclose a two terminal device in which the terminals are separated by a chalcogenide body, where the electrical properties of the chalcogenide material provide switching behavior. The switching behavior of the device disclosed in Klersy, et al. is controlled by the voltage applied to the chalcogenide body through a first terminal. When enough voltage is applied, the chalcogenide body switches from a non-conductive state to a conductive state allowing current to flow from the first terminal through the chalcogenide body to a second terminal. The Klersy, et al. device, contrary to Appellants' claimed bipolar transistor, has only two states of conduction, where the device does not conduct or is highly conductive depending on the voltage applied to the chalcogenide body. The Klersy, et al. device is far removed from Appellants' claimed bipolar transistor.

Appellants' claimed bipolar transistor and the chalcogenide switching device disclosed in Klersy, et al., similar to the technology discussed by the Federal Circuit in *Wang Laboratories, Inc. v. Toshiba Corp.*, have a substantially different structure and substantially different functionality indicating that the applied reference and Appellants' claimed structure

pertain to non-analogous art. Therefore, since the applied reference pertains to non-analogous art, there is no motivation to modify AAPA with the passivation layer disclosed in Klersy et al. in a manner to produce applicants' claimed bipolar transistor structure.

Appellants' further note that Klersy, et al. is not reasonably pertinent to the problem in which Appellants' were concerned. Appellants' disclose that the positioning of the passivation layer on the exposed sidewalls of the emitter reduces the incidence of emitter/base shorts formed during silicidation of the exposed surfaces of the bipolar transistor. Shorting the emitter region to the base region produces a transistor that will not switch on, because when the emitter region and base region are in intimate electrical contact the potential of the base region cannot be greater than the emitter region. Therefore, shorting the base and emitter produces a device that does not provide current flow.

In addition to failing to teach or suggest a bipolar transistor including an emitter region, Klersy, et al. also fail to disclose silicide formation or the incidence of silicide shorts resulting in a device that will not switch on. The short circuit disclosed in Klersy, et al. occurs where the chalcogenide body is bypassed through a low resistance conduction path introduced by contamination from the first and second terminals. Opposite the problem in which Appellants' were concerned, current flow that bypasses the chalcogenide body produces a device that is effectively switched on resulting in an uncontrolled high current between the terminals. Therefore, since the problem considered by Klersy, et al., where a short circuit results in a device with an uncontrolled high current flow, is opposite the problem considered by Appellants, where a short produces a device that will not switch on and will not flow current, Klersy, et al. are not reasonably pertinent to the problem in which Appellants' were concerned. Since Klersy, et al. are not pertinent to the problem in which

Appellants' were concerned, there is no motivation to modify or combine the passivation layer disclosed in Klersy, et al. in a manner to produce Appellants' claimed structure.

In addition to being non-analogous art, modifying the passivation layer disclosed in Klersy, et al. would change the principal of operation of the Klersy, et al. passivation layer. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)

Contrary to Appellants' invention, in which the permanent passivation layer is formed prior to silicidation, Klersy, et al. disclose forming the passivation layer over the entire transistor in order to protect the transistor from the environment and unintended contact with other devices and circuits. In order to protect the transistor from other devices, the entire transistor must be encapsulated by the passivation layer. Modifying the passivation layer disclosed in Klersy, et al. to be positioned only on the emitter sidewalls to allow for silicidation of the emitter and SiGe body, as taught by Appellants, would degrade the passivation layers ability to protect the Klersy, et al. device from the environment and unintended contact with other devices and circuits. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no motivation to make the proposed modification. *See In re Gordan*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)

The forgoing remarks clearly demonstrate that there is no suggestion or motivation, either in the applied references themselves or the knowledge generally available to one of ordinary skill in the art, to modify the combined disclosures of the AAPA, Klersy, et al. and

Sedra and Smith to produce Appellants' claimed heterojunction transistor or fabrication method.

In view of the above remarks, Appellants respectfully submit Claims 1, 9, 13, 14, 15 and 18, on appeal, are not obvious over the combined disclosures of the AAPA, Klersy, et al., and Sedra and Smith.

II. The combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 6,331,492 to Misium, et al. ("Misium, et al.") do not render Claims 2 and 5-8, on appeal, unpatentable under 35 U.S.C. §103(a).

Before addressing the specific grounds for rejection of Claims 2 and 5-8, Appellants observe that the Examiner referred to a Hasegawa reference, which is not of record in the present case. Appellants have repeatedly requested that the Examiner clarify which references are being referred to. It appears from the Examiner's comments that the Examiner meant to recite Klersy, et al. instead of Hasegawa. Thus, this rejection has been treated as if Klersy, et al. was one of the applied references.

Claims 2 and 5-8 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over the combination of the AAPA, Klersy, et al., Sedra and Smith, and Misium, et al. Claims 2 and 5-8 are dependent on independent Claim 1. If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Appellants submit that the AAPA, Klersy, et al. and Sedra and Smith fail to teach or suggest Appellants' method of improving the SiGe bipolar yield of a SiGe heterojunction bipolar transistor, as recited in Claims 2 and 5-8. Appellants' respectfully submit that the above remarks, concerning the deficiencies of the AAPA, Klersy, et al. and Sedra and Smith to render Claims 1, 9, 13, 14, 15 and 18 unpatentable, apply equally well to this obviousness rejection of Claims 2 and 5-8, under 35 U.S.C. §103. Therefore the remarks from Section I of this brief are incorporated by reference.

Misium, et al. do not fulfill the deficiencies of the combined disclosures of AAPA, Klersy, et al., and Sedra and Smith. Misium, et al., referring to Col. 3 lines 49-53, relate to a process for rending a silicon dioxide layer resistant to etch chemistries used in integrated circuit component manufacturing, such as HF. Misium, et al. fail to teach or suggest that by forming a permanent passivation layer on the emitter prior to silicidation one can prevent the bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%, as recited in Claims 1, 9 and 18.

In view of the above remarks, Appellants respectfully submit that Claims 2 and 5-8, on appeal, are patentable subject matter over the combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and Misium, et al.

III. The combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 4,987,102 to Nguyen, et al. ("Nguyen, et al.") do not render Claims 3, 4, 16, and 17, on appeal, unpatentable under 35 U.S.C. §103(a).

Before addressing the specific grounds for rejection of Claims 3, 4, 16, and 17, Appellants observe that the Examiner has again referred to a Hasegawa reference, which is not of record in the present case. It appears from the Examiner's comments that the Examiner meant to recite Klersy, et al. instead of Hasegawa. Thus, this rejection has also been treated as if Klersy, et al. was one of the applied references.

Claims 3, 4, 16, and 17 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over the combination of the AAPA, Klersy, et al., Sedra and Smith, and Nguyen, et al. Claims 3 and 4 are dependent on independent Claim 1 and Claims 16 and 17 are dependent on Claim 9. If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Appellants submit that AAPA, Klersy, et al. and Sedra and Smith fail to teach or suggest Appellants' SiGe heterojunction bipolar transistor or fabrication method, as recited in Claims 3, 4, 16, and 17. Appellants' respectfully submit that the above remarks, concerning the deficiencies of the AAPA, Klersy, et al. and Sedra and Smith to render Claims 1, 9, 13, 14, 15 and 18 unpatentable, apply equally well to this obviousness rejection of Claims 3, 4, 16, and 17, under 35 U.S.C. §103. Therefore the remarks from Section I of this brief are incorporated by reference.

Nguyen, et al. do not fulfill the deficiencies of the combined disclosures of AAPA, Klersy, et al., Sedra and Smith. Nguyen, et al. disclose a method for forming high purity thin films on a semiconductor substrate, where the preferred method of thin film deposition is

plasma enhanced chemical vapor deposition. Nguyen, et al. fail to teach or suggest that by forming a permanent passivation layer on the emitter prior to silicidation one can prevent the bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.

In view of the above remarks, Appellants respectfully submit that Claims 3, 4, 16, and 17, on appeal, are patentable subject matter over the combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and Nguyen, et al.

IV. The combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 4,757,027 to Vora ("Vora") do not render Claims 10 and 11, on appeal, unpatentable under 35 U.S.C. §103(a).

Before addressing the specific grounds for rejection of Claims 10 and 11, Appellants again note that the Examiner referred to a Hasegawa reference, which is not of record in the present case. It appears from the Examiner's comments however that the Examiner meant to recite Klersy, et al. instead of Hasegawa. Thus, this rejection has also been treated as if Klersy, et al. was one of the applied references.

Claims 10 and 11 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over the combination of the AAPA, Klersy, et al., Sedra and Smith, and Vora. Claims 10 and 11 are dependent on independent Claim 9. If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). "To establish a prima facie case of obviousness of a

claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Appellants submit that AAPA, Klersy, et al., Sedra and Smith and Vora fail to teach or suggest Appellants' SiGe heterojunction bipolar transistor, as recited in Claims 10 and 11. Appellants' respectfully submit that the above remarks, concerning the deficiencies of the AAPA, Klersy, et al. and Sedra and Smith to render Claims 1, 9, 13, 14, 15 and 18 unpatentable, apply equally well to this obviousness rejection of Claims 10 and 11, under 35 U.S.C. §103. Therefore the remarks from Section I of this brief are incorporated by reference.

Vora does not fulfill the deficiencies of the combined disclosures of AAPA, Klersy, et al., and Sedra and Smith. Vora relates to techniques for making vertical transistor structures in islands of an epitaxial silicon layer. Vora fails to teach or suggest that by forming a permanent passivation layer on the emitter prior to silicidation one can *prevent the bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.*

In view of the above remarks, Appellants respectfully submit that Claims 10 and 11, on appeal, are patentable subject matter over the combined disclosures of AAPA, Klersy, et al., Sedra and Smith, and Vora.

V. The combined disclosures of AAPA, Sedra and Smith, and U.S. Patent No. 6,268,779 to Van Zeijl ("Van Zeijl") do not render Claim 12, on appeal, unpatentable under 35 U.S.C. §103(a).

Appellants again note that, similar to the rejection of Claims 2 and 5-8, the Examiner referred to a Hasegawa reference, which is not of record in the present case. The rejections have been treated as if Klersy, et al. was one of the applied references.

Claim 12 stands rejected under 35 U.S.C. §103(a) as allegedly unpatentable over the combination of the AAPA, Klersy, et al., Sedra and Smith, and Van Zeijl. Claim 12 is dependent on independent Claim 9. If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Appellants submit that AAPA, Klersy, et al., Sedra and Smith and Van Zeijl fail to teach or suggest Appellants' SiGe heterojunction bipolar transistor, as recited in Claim 12. Appellants' respectfully submit that the above remarks, concerning the deficiencies of the AAPA, Klersy, et al. and Sedra and Smith to render Claims 1, 9, 13, 14, 15 and 18 unpatentable, apply equally well to this obviousness rejection of Claim 12, under 35 U.S.C. §103. Therefore the remarks from Section I of this brief are incorporated by reference.

Van Zeijl does not fulfill the deficiencies of the combined disclosures of AAPA, Klersy, et al., and Sedra and Smith. Van Zeijl relates to an integrated voltage controlled oscillator including varactors and fixed capacitors in a stacked arrangement, where the stacked arrangement decreases the surface area required for implementation of the device. There is no teaching or suggestion in Van Zeijl that by forming a permanent passivation layer on the emitter prior to silicidation one can *prevent the bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%*

9. Conclusion

The above arguments establish that all of the claims on appeal are enabled, definite and patentable over the substantive grounds of rejection raised in the Final Rejection. Appellants therefore respectfully request that the substantive grounds used in rejecting Claims 1-18, on appeal, made by the Examiner, be reversed by the Broad of Patent Appeals and Interferences.

Respectfully submitted,

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APPENDIX

10. The claims on appeal for U.S. Application Serial No. 09/773,798 filed February 1, 2001.

1. A method of fabricating a SiGe heterojunction bipolar transistor comprising the steps of:

providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls;

forming a permanent passivation layer on said exposed sidewalls of said emitter, said insulator layer and portions of said SiGe base region; and

siliciding exposed silicon surfaces of at least said emitter and said SiGe base region not protected by said permanent passivation layer to form silicide regions therein, wherein said permanent passivation layer prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.

2. The method of Claim 1 wherein said passivation layer is formed from a rapid thermal chemical vapor deposition process.

3. The method of Claim 1 wherein said passivation layer is composed of a nitride, an oxide, an oxynitride or any combination thereof.

4. The method of Claim 1 wherein said passivation layer is a nitride passivation layer.

5. The method of Claim 4 wherein said nitride passivation layer is formed from a rapid thermal chemical vapor deposition process which is carried out in a nitrogen-containing atmosphere.

6. The method of Claim 5 wherein said nitrogen-containing atmosphere is selected from the group consisting of NO, N_2O and N_2.

7. The method of Claim 2 wherein said rapid thermal chemical vapor deposition process is carried out at a temperature of about 700°C or greater.

8. The method of Claim 1 wherein said SiGe base region is formed by a deposition process selected from the group consisting of ultra-high vacuum chemical vapor deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD) and plasma-enhanced chemical vapor deposition.

9. A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a permanent conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and a portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said permanent conformal passivation layer, wherein said permanent passivation layer prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.

10. The SiGe heterojunction bipolar transistor of Claim 9 wherein said semiconductor substrate is selected from the group consisting of Si, Ge, SiGe, GaAs, InAs, InP, other III/V compound semiconductors, Si/Si and Si/SiGe.

11. The SiGe heterojunction bipolar transistor of Claim 9 wherein said emitter is composed of intrinsic polysilicon.

12. The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned insulator is composed of SiO_2 or Si oxynitride.

13. The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned insulator is composed of multi-insulator layers.

14. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is also formed on vertical sidewalls of said patterned insulator and portions of said SiGe base region.

15. The SiGe heterojunction bipolar transistor of Claim 9 wherein said silicide regions are formed in an exposed horizontal surface of said emitter, said polycrystalline Si region and a portion of said SiGe base region.

16. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is composed of a nitride, an oxide, an oxynitride or any combination thereof.

17. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is a nitride passivation layer.

18. A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a permanent conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and an inclined portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said permanent conformal passivation layer, wherein said permanent passivation layer prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.